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(72) Inventors:
 • **WASAKI, Masaru** TDK Corporation
 Tokyo 103-8272 (JP)
 • **SAITOH, Yoshihiro** TDK Corporation
 Tokyo 103-8272 (JP)

(71) Applicant: **TDK Corporation**
 Chuo-ku, Tokyo 103-8272 (JP)

(74) Representative: **Grünecker, Kinkeldey,
 Stockmair & Schwanhäusser** Anwaltssozietät
 Maximilianstrasse 58
 80538 München (DE)

(54) **COMMON MODE SIGNAL SUPPRESSING CIRCUIT AND NORMAL MODE SIGNAL SUPPRESSING CIRCUIT**

(57) A common mode signal suppressing circuit comprises: a first winding (11) inserted to a conductor line (3); a second winding (12) that is inserted to a conductor line (4) and coupled to the first winding (11) through a magnetic core (10) and that suppresses common mode signals in cooperation with the first winding (11); and a third winding (13) coupled to the first and second windings (11, 12) through the core (10). The

common mode signal suppressing circuit further comprises a phase-inverted signal transmitting circuit (15) connected to the third winding (13) and to the conductor lines (3, 4). The phase-inverted signal transmitting circuit (15) detects a common mode signal on the conductor lines (3, 4), and supplies a phase-inverted signal to the third winding (13), the phase-inverted signal having a phase opposite to the phase of the common mode signal.

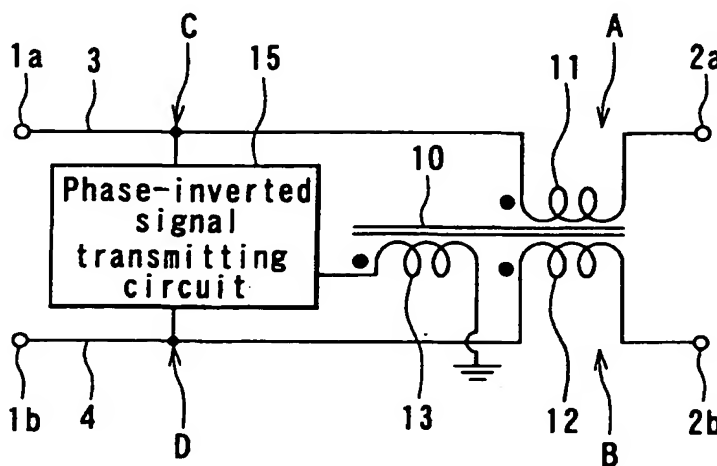


FIG. 1

Description

TECHNICAL FIELD

[0001] The present invention relates to a common mode signal suppressing circuit for suppressing common mode signals with identical phases propagating through two conductor lines and to a normal mode signal suppressing circuit for suppressing normal mode signals transmitted by conductor lines.

BACKGROUND ART

[0002] Power electronics apparatuses such as a switching power supply, an inverter and a lighting circuit of a lighting fixture incorporate a power transformer circuit for transforming power. The power transformer circuit incorporates a switching circuit for transforming a direct current to an alternating current having rectangular waves. Consequently, the power transformer circuit develops a ripple voltage having a frequency equal to the switching frequency of the switching circuit, and noise resulting from the switching operation of the switching circuit. Such a ripple voltage and noise affect other apparatuses. It is therefore required to provide a means for reducing the ripple voltage and noise between the power transformer circuit and the other apparatuses or lines.

[0003] LC filters, that is, filters each incorporating an inductance element (an inductor) and a capacitor, are often used as a means for reducing a ripple voltage and noise. The LC filters include a T filter and a π filter, in addition to the one incorporating an inductance element and a capacitor. A typical noise filter for suppressing electromagnetic interference (EMI) is a type of LC filters, too. A typical EMI filter is made up of a combination of discrete elements such as a common mode choke coil, a normal mode choke coil, an X capacitor, and a Y capacitor.

[0004] Recently, power line communications have been developed as a potential communications technique used for creating a communications network at home. Through the power line communications, high-frequency signals are superimposed on a power line to perform communications.

When the power line communications are performed, noise emerges on the power line because of the operations of various electric and electronic apparatuses connected to the power line, which causes a reduction in quality of communications, such as an increase in error rate. It is therefore required to provide a means for reducing noise on the power line. Moreover, it is required for the power line communications to prevent communications signals on an indoor power line from leaking to an outdoor power line. The LC filters are used as a means for reducing noise on the power line and for preventing communications signals on the indoor power line from leaking to the outdoor power line as thus de-

scribed, too.

[0005] There are two types of noise propagating along two conductor lines: one is normal mode noise that creates a potential difference between the two conductor lines, while the other is common mode noise that propagates along the two conductor lines with identical phases.

[0006] FIG. 17 illustrates an example of configuration of an LC filter for reducing common mode noise. The LC filter comprises: a pair of terminals 201a and 201b; another pair of terminals 202a and 202b; a common mode choke coil 203 provided between the terminals 201a, 201b and the terminals 202a, 202b; a capacitor 204 having an end connected to the terminal 201a and the other end grounded; and a capacitor 205 having an end connected to the terminal 201b and the other end grounded.

[0007] The common mode choke coil 203 has one magnetic core 203a and two windings 203b and 203c wound around the core 203a. The winding 203b has an end connected to the terminal 201a and the other end connected to the terminal 202a. The winding 203c has an end connected to the terminal 201b and the other end connected to the terminal 202b. The windings 203b and 203c are wound around the core 203a in such directions that, when magnetic fluxes are induced in the core 203a by currents flowing through the windings 203b and 203c when a normal mode current is fed to the windings 203b and 203c, these fluxes are cancelled out by each other.

[0008] The LC filter of FIG. 17 is inserted somewhere along the two conductor lines for transmitting power. The terminals 201a and 202a are connected to one of the conductor lines while the terminals 201b and 202b are connected to the other one of the conductor lines.

[0009] Next, FIG. 18 illustrates an example of configuration of an LC filter for reducing normal mode noise. The LC filter comprises: a pair of terminals 301a and 301b; another pair of terminals 302a and 302b; a coil 303 as an inductance element; and a capacitor 304. The terminal 302b is connected to the terminal 301b. The coil 303 has an end connected to the terminal 301a and the other end connected to the terminal 302a. The capacitor 304 has an end connected to the other end of the coil 303 and to the terminal 302a. The capacitor 304 has the other end connected to the terminals 301b and 302b.

[0010] The LC filter of FIG. 18 is inserted somewhere along the two conductor lines for transmitting power. The terminals 301a and 302a are connected to one of the conductor lines while the terminals 301b and 302b are connected to the other one of the conductor lines.

[0011] The Published Unexamined Japanese Patent Application Heisei 9-102723 (1997) discloses a line filter using a transformer. The line filter comprises the transformer and a filter circuit. The transformer incorporates a secondary winding inserted to one of two conductor lines for transmitting power from an alternating power supply to a load. The filter circuit has two inputs con-

nected to ends of the alternating power supply, and two outputs connected to ends of a primary winding of the transformer. In the line filter, the filter circuit extracts noise components from the supply voltage and supplies the noise components to the primary winding of the transformer, so that the noise components are subtracted from the supply voltage on the conductor line to which the secondary winding of the transformer is inserted. The line filter reduces normal mode noise.

[0012] The conventional LC filters have a problem that, since the filters have a specific resonant frequency determined by the inductance and the capacitance, a desired amount of attenuation is obtained only within a narrow frequency range.

[0013] For the filter inserted to the conductor line for transmitting power, it is required that desired characteristics be obtained while the current for transmitting power is fed, and that a measure for coping with a rise in temperature be provided. Therefore, such a filter has a problem that the inductance element is increased in size for implementing the desired characteristics.

[0014] According to the line filter disclosed in the Published Unexamined Japanese Patent Application Heisei 9-102723, it is theoretically possible to remove noise components completely as long as the impedance of the filter circuit is zero and the coupling coefficient of the transformer is 1. In practice, however, it is impossible that the impedance of the filter circuit is zero, and furthermore, the impedance changes in response to the frequency. In particular, if the filter circuit is made up of a capacitor, a series resonant circuit is made up of the capacitor and the primary winding of the transformer. Therefore, the impedance of the signal path including the capacitor and the primary winding of the transformer is reduced only in a narrow frequency range around the resonant frequency of the series resonant circuit. As a result, the line filter is capable of removing noise components only in a narrow frequency range. In addition, the coupling coefficient of the transformer is smaller than 1 in practice. Therefore, the noise components supplied to the primary winding of the transformer will not be completely subtracted from the supply voltage. Because of these reasons, the line filter actually designed has a problem that it is not capable of effectively reducing noise components in a wide frequency range.

DISCLOSURE OF THE INVENTION

[0015] It is a first object of the invention to provide a common mode signal suppressing circuit for effectively suppressing common mode signals in a wide frequency range and for achieving a reduction in size.

[0016] It is a second object of the invention to provide a normal mode signal suppressing circuit for effectively suppressing normal mode signals in a wide frequency range and for achieving a reduction in size.

[0017] A common mode signal suppressing circuit of the invention is a circuit for suppressing common mode

signals propagating with identical phases through two conductor lines. The common mode signal suppressing circuit comprises: a first winding inserted to one of the conductor lines at a specific first point; a second winding that is inserted to the other of the conductor lines at a second point corresponding to the first point and is coupled to the first winding, the second winding suppressing the common mode signals in cooperation with the first winding; a third winding coupled to the first and second windings such that a mutual inductance is generated between the third winding and the first and second windings; and a phase-inverted signal transmitting means connected to the third winding and to the one of the conductor lines at a third point different from the first point, the transmitting means being further connected to the other of the conductor lines at a fourth point corresponding to the third point and different from the second point, the transmitting means transmitting a phase-inverted signal for suppressing the common mode signals.

[0018] In the common mode signal suppressing circuit of the invention, when a source of the common mode signals is located at a point closer to the third and fourth points than the first and second points except a point between the first and third points and a point between the second and fourth points, the transmitting means detects a common mode signal and supplies the phase-inverted signal to the third winding, the phase-inverted signal having a phase opposite to a phase of the common mode signal detected. In addition, the third winding injects the phase-inverted signal to the two conductor lines through the first and second windings. As a result, the common mode signal is suppressed on portions of the two conductor lines from the first and second points onward along the direction of travel of the common mode signal.

[0019] In the common mode signal suppressing circuit of the invention, when the source of the common mode signals is located at a point closer to the first and second points than the third and fourth points except a point between the first and third points and a point between the second and fourth points, the third winding detects a common mode signal, and the transmitting means injects the phase-inverted signal to the two conductor lines, the phase-inverted signal having a phase opposite to the phase of the common mode signal detected by the third winding. As a result, the common mode signal is suppressed on portions of the two conductor lines from the third and fourth points onward along the direction of travel of the common mode signal.

[0020] The common mode signal suppressing circuit of the invention may further comprise an impedance element provided on the two conductor lines at a point between the first and third points and a point between the second and fourth points, the impedance element reducing the peak value of a common mode signal passing therethrough.

[0021] In the common mode signal suppressing circuit of the invention, the phase-inverted signal transmit-

ting means may incorporate a high-pass filter for allowing a common mode signal to pass therethrough. The high-pass filter may incorporate a capacitor.

[0022] In the common mode signal suppressing circuit of the invention, the impedance element may incorporate: a fourth winding inserted to one of the conductor lines; and a fifth winding that is inserted to the other of the conductor lines and coupled to the fourth winding and that suppresses the common mode signals in cooperation with the fourth winding. Each of the fourth and fifth windings may have an inductance of 0.3 μ H or greater.

[0023] In the common mode signal suppressing circuit of the invention, the coupling coefficient between the third winding and the first and second windings may be 0.7 or greater.

[0024] A normal mode signal suppressing circuit of the invention is a circuit for suppressing normal mode signals transmitted by two conductor lines and creating a potential difference between the two conductor lines. The normal mode signal suppressing circuit comprises: a first inductance element inserted to one of the conductor lines at a specific first point; a second inductance element coupled to the first inductance element such that a mutual inductance is generated between the first and second inductance elements; a phase-inverted signal transmitting means connected to the second inductance element and to the one of the conductor lines at a second point different from the first point, the transmitting means transmitting a phase-inverted signal for suppressing the normal mode signals; and an impedance element provided on the one of the conductor lines at a point between the first and second points, the impedance element reducing a peak value of a normal mode signal passing therethrough.

[0025] In the normal mode signal suppressing circuit of the invention, when a source of the normal mode signals is located at a point closer to the second point than the first point except a point between the first and second points, the transmitting means detects a normal mode signal and supplies the phase-inverted signal to the second inductance element, the phase-inverted signal having a phase opposite to the phase of the normal mode signal detected. In addition, the second inductance element injects the phase-inverted signal to the one of the conductor lines through the first inductance element. As a result, the normal mode signal is suppressed on a portion of the one of the conductor lines from the first point onward along the direction of travel of the normal mode signal.

[0026] In the normal mode signal suppressing circuit of the invention, when the source of the normal mode signals is located at a point closer to the first point than the second point except a point between the first and second points, the second inductance element detects a normal mode signal, and the transmitting means injects the phase-inverted signal to the one of the conductor lines, the phase-inverted signal having a phase op-

posite to a phase of the normal mode signal detected by the second inductance element. As a result, the normal mode signal is suppressed on a portion of the one of the conductor lines from the second point onward along the direction of travel of the normal mode signal.

[0027] In the normal mode signal suppressing circuit of the invention, the impedance element reduces the peak value of the normal mode signal passing therethrough, which reduces the difference between the peak value of the normal mode signal propagating via the impedance element and the peak value of the phase-inverted signal injected to the one of the conductor lines via the phase-inverted signal transmitting means.

[0028] In the normal mode signal suppressing circuit of the invention, the phase-inverted signal transmitting means may incorporate a high-pass filter for allowing a normal mode signal to pass therethrough. The high-pass filter may incorporate a capacitor. The high-pass filter may incorporate a plurality of capacitors that are combined.

[0029] In the normal mode signal suppressing circuit of the invention, the impedance element may incorporate a third inductance element inserted to the one of the conductor lines. The third inductance element may have an inductance of 0.3 μ H or greater.

[0030] In the normal mode signal suppressing circuit of the invention, the coupling coefficient between the first and second inductance elements may be 0.7 or greater.

[0031] Other and further objects, features and advantages of the invention will appear more fully from the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]

FIG. 1 is a schematic diagram illustrating a basic configuration of a common mode signal suppressing circuit of a first embodiment of the invention.

FIG. 2 is a schematic diagram illustrating a specific example of configuration of the common mode signal suppressing circuit of FIG. 1.

FIG. 3 is a schematic diagram for illustrating the principle of suppression of common mode signals by the common mode signal suppressing circuit of the first embodiment of the invention.

FIG. 4 is a schematic diagram for illustrating the operation of the common mode signal suppressing circuit of the first embodiment of the invention.

FIG. 5 is a schematic diagram illustrating a basic configuration of a common mode signal suppressing circuit of a second embodiment of the invention.

FIG. 6 is a schematic diagram illustrating a specific example of configuration of the common mode signal suppressing circuit of FIG. 5.

FIG. 7 is a schematic diagram for illustrating the operation of the common mode signal suppressing circuit

cuit of the second embodiment of the invention.

FIG. 8 is a plot showing frequency characteristics of gains obtained by simulation for a reference circuit and the common mode signal suppressing circuit of FIG. 6.

FIG. 9 is a plot showing frequency characteristics of gains obtained by simulation for the reference circuit and the common mode signal suppressing circuit of FIG. 6.

FIG. 10 is a schematic diagram illustrating a basic configuration of a normal mode signal suppressing circuit of a third embodiment of the invention.

FIG. 11 is a schematic diagram illustrating a specific example of configuration of the normal mode signal suppressing circuit of FIG. 10.

FIG. 12 is a schematic diagram illustrating the configuration of FIG. 11 from which the third inductance element is removed.

FIG. 13 is a schematic diagram illustrating a circuit made up of the normal mode signal suppressing circuit of FIG. 11 to which a normal mode signal source and a load are connected.

FIG. 14 is a plot showing frequency characteristics of gains obtained by simulation for a reference circuit and the normal mode signal suppressing circuit of FIG. 11.

FIG. 15 is a plot showing frequency characteristics of gains obtained by simulation for the reference circuit and the normal mode signal suppressing circuit of FIG. 11.

FIG. 16 is a schematic diagram illustrating a configuration of a normal mode signal suppressing circuit of a fourth embodiment of the invention.

FIG. 17 is a schematic diagram illustrating an example of configuration of an LC filter for reducing common mode noise.

FIG. 18 is a schematic diagram illustrating an example of configuration of an LC filter for reducing normal mode noise.

BEST MODE FOR CARRYING OUT THE INVENTION

[0033] Preferred embodiments of the invention will now be described in detail with reference to the accompanying drawings.

[First Embodiment]

[0034] FIG. 1 is a schematic diagram illustrating a basic configuration of a common mode signal suppressing circuit of a first embodiment of the invention. The common mode signal suppressing circuit of the embodiment comprises a pair of terminals 1a and 1b, another pair of terminals 2a and 2b, a conductor line 3 connecting the terminals 1a and 2a to each other, and a conductor line 4 connecting the terminals 1b and 2b to each other. The common mode signal suppressing circuit is designed to be connected to a power line for transmitting alternating

current power or direct current power. The power line includes two power conductor lines. The common mode signal suppressing circuit is designed to be inserted somewhere along the two power conductor lines. The terminals 1a and 2a are connected to one of the power conductor lines while the terminals 1b and 2b are connected to the other of the power conductor lines. A source of common mode signals to be suppressed by the common mode signal suppressing circuit is connected to the terminals 1a and 1b or the terminals 2a and 2b. Therefore, the common mode signals to be suppressed are inputted to the common mode signal suppressing circuit from the terminals 1a and 1b or the terminals 2a and 2b.

[0035] Here, the common mode signals are signals propagating through the two power conductor lines with identical phases. The common mode signals to be suppressed include noise and unwanted communications signals.

[0036] The common mode signal suppressing circuit further comprises: a first winding 11 inserted to the conductor line 3 at a specific first point A; a second winding 12 that is inserted to the conductor line 4 at a second point B corresponding to the first point A and is coupled to the first winding 11 through a magnetic core 10 and that suppresses common mode signals in cooperation with the first winding 11; and a third winding 13 coupled to the first winding 11 and the second winding 12 through the core 10 such that a mutual inductance is generated between the third winding 13 and the first and second windings 11, 12. For example, the numbers of turns of the windings 11, 12 and 13 may be equal. The core 10, the first winding 11 and the second winding 12 make up a common mode choke coil. That is, the windings 11 and 12 are wound around the core 10 in such directions that, when magnetic fluxes are induced in the core 10 by currents flowing through the windings 11 and 12 when a normal mode current is fed to the windings 11 and 12, these fluxes are cancelled out by each other. The windings 11 and 12 thereby suppress common mode signals and allow normal mode signals to pass.

[0037] The common mode signal suppressing circuit further comprises a phase-inverted signal transmitting circuit 15 connected to the third winding 13 and to the conductor line 3 at a third point C different from the first point A, and furthermore, to the conductor line 4 at a fourth point D corresponding to the third point C and different from the second point B. The phase-inverted signal transmitting circuit 15 transmits phase-inverted signals for suppressing common mode signals. The phase-inverted signal transmitting circuit 15 has first to third terminals. The first terminal is connected to the conductor line 3 at the third point C. The second terminal is connected to the conductor line 4 at the fourth point D. The third terminal is connected to an end of the third winding 13. The other end of the third winding 13 is grounded. The phase-inverted signal transmitting circuit 15 corresponds to the phase-inverted signal transmit-

ting means of the invention.

[0038] FIG. 2 is a schematic diagram illustrating a specific example of configuration of the common mode signal suppressing circuit of FIG. 1. In this example, the phase-inverted signal transmitting circuit 15 is made up of a high-pass filter 15A for allowing signals having a specific frequency or higher to pass among common mode signals or phase-inverted signals. The high-pass filter 15A includes capacitors 51 and 52. The capacitor 51 has an end connected to the conductor line 3 at the point C. The capacitor 52 has an end connected to the conductor line 4 at the point D. The other end of each of the capacitors 51 and 52 is connected to an end of the third winding 13.

[0039] The operation of the common mode signal suppressing circuit of the embodiment will now be described. First, the operation of the common mode signal suppressing circuit will be described, wherein the common mode signal source is located at a point closer to the third and fourth points C and D than the first and second points A and B except a point between the first point A and the third point C and a point between the second point B and the fourth point D. In this case, the phase-inverted signal transmitting circuit 15 detects a common mode signal at the third and fourth points C and D, and supplies a phase-inverted signal to the third winding 13, the phase-inverted signal having a phase opposite to the phase of the common mode signal detected. The third winding 13 injects the phase-inverted signal to the two conductor lines 3 and 4 at the first and second points A and B through the first winding 11 and the second winding 12. As a result, the common mode signal is suppressed on portions of the two conductor lines 3 and 4 from the first and second points A and B onward, respectively, along the direction of travel of the common mode signal.

[0040] Next, the operation of the common mode signal suppressing circuit will be described, wherein the common mode signal source is located at a point closer to the first and second points A and B than the third and fourth points C and D except a point between the first point A and the third point C and a point between the second point B and the fourth point D. In this case, the third winding 13 detects a common mode signal on the conductor lines 3 and 4 at the first and second points A and B. The phase-inverted signal transmitting circuit 15 injects a phase-inverted signal to the two conductor lines 3 and 4 at the third and fourth points C and D, the phase-inverted signal having a phase opposite to the phase of the common mode signal detected by the third winding 13. As a result, the common mode signal is suppressed on portions of the two conductor lines 3 and 4 from the third and fourth points C and D onward, respectively, along the direction of travel of the common mode signal.

[0041] Reference is now made to FIG. 3 to describe the principle of suppression of common mode signals by the common mode signal suppressing circuit of the

embodiment. Here, a case will be described, wherein the common mode signal source is located at a point closer to the third and fourth points C and D than the first and second points A and B. FIG. 3 illustrates the common mode signal suppressing circuit having a configuration similar to that of FIG. 2. In the following description, it is assumed that the impedance of the high-pass filter 15A (the capacitors 51 and 52) is zero, the numbers of turns of the windings 11 to 13, for example, are equal, and the coupling coefficient between the winding 13 and the windings 11 and 12 is 1.

[0042] It is assumed that, in the common mode signal suppressing circuit of FIG. 3, a common mode signal that creates a potential difference V_{in1} in the potential of the ground GND is inputted to the terminals 1a and 1b. If the common mode signal has a frequency within the pass band of the high-pass filter 15A, the common mode signal passes through the high-pass filter 15A, and a phase shift of 180 degrees occurs at the same time by means of the operation of the capacitors 51 and 52. As a result, a potential difference $-V_{in1}$ is created between the ends of the third winding 13. A potential difference $-V_{in1}$ is also created between the ends of the first winding 11 and between the ends of the second winding 12, in accordance with the potential difference $-V_{in1}$ created between the ends of the third winding 13. This is expressed by the equation below where the difference between the potential of the ground GND and the potential of the terminals 2a and 2b is V_{o1} .

$$V_{o1} = V_{in1} + (-V_{in1}) = 0$$

[0043] According to the common mode signal suppressing circuit of FIG. 3 as thus described, as long as the impedance of the high-pass filter 15A is zero and the coupling coefficient between the winding 13 and the windings 11 and 12 is 1, it is possible to completely remove common mode signals at any frequency within the pass band of the high-pass filter 15A. In practice, however, it is impossible that the impedance of the high-pass filter 15A is zero. In addition, the coupling coefficient between the winding 13 and the windings 11 and 12 is smaller than 1. Therefore, the common mode signal suppressing circuit of FIG. 3 is not capable of removing common mode signals completely. Nevertheless, according to the embodiment, it is possible to implement the common mode signal suppressing circuit that is capable of effectively suppressing common mode signals in a wide frequency range and that has a simple configuration to achieve a reduction in size.

[0044] Reference is now made to FIG. 4 to describe details of the operation of the common mode signal suppressing circuit of the embodiment. FIG. 4 illustrates a portion of the common mode signal suppressing circuit of FIG. 2 that relates to suppression of signals passing through the conductor line 3. The circuit of FIG. 4 incorporates the terminals 1a and 2a, the first winding 11, the

third winding 13 and the capacitor 51. A common mode signal source 21 and a load 22 are connected to the circuit of FIG. 4. The common mode signal source 21 is connected between the terminal 1a and the ground GND, and creates a potential difference V_{in1} between the terminal 1a and the ground GND. The load 22 is connected between the terminal 2a and the ground GND, and has an impedance Z_{o1} .

[0045] In the circuit of FIG. 4, the inductance of the third winding 13 is L_{11} , the inductance of the first winding 11 is L_{12} , and the capacitance of the capacitor 51 is C_{11} . The current passing through the capacitor 51 and the third winding 13 is ' i_{11} ', and the sum of impedances on the path of the current i_{11} is Z_1 . The current passing through the first winding 11 is ' i_{12} ', and the sum of impedances on the path of the current i_{12} is Z_2 .

[0046] The mutual inductance between the first winding 11 and the third winding 13 is M , and the coupling coefficient between the first winding 11 and the third winding 13 is K . The coupling coefficient K is expressed by the following equation (1).

$$K = M/\sqrt{L_{11} \cdot L_{12}} \quad (1)$$

[0047] The above-mentioned sums Z_1 and Z_2 of impedances are expressed by the following equations (2) and (3), respectively, where ' j ' indicates $\sqrt{-1}$, and ' ω ' indicates the angular frequency of the common mode signal.

$$Z_1 = j(\omega L_{11} - 1/\omega C_{11}) \quad (2)$$

$$Z_2 = Z_{o1} + j\omega L_{12} \quad (3)$$

[0048] The potential difference V_{in1} is expressed by the following equations (4) and (5).

$$V_{in1} = Z_1 \cdot i_{11} + j\omega M \cdot i_{12} \quad (4)$$

$$V_{in1} = Z_2 \cdot i_{12} + j\omega M \cdot i_{11} \quad (5)$$

[0049] Based on the equations (2) to (5), an equation that expresses the current ' i_{12} ' without including the current ' i_{11} ' will be obtained below. First, the following equation (6) is obtained from the equation (4).

$$i_{11} = (V_{in1} - j\omega M \cdot i_{12})/Z_1 \quad (6)$$

[0050] Next, the equation (6) is substituted into the equation (5), and the following equation (7) is thereby obtained.

$$i_{12} = V_{in1}(Z_1 - j\omega M)/(Z_1 \cdot Z_2 + \omega^2 \cdot M^2) \quad (7)$$

[0051] To suppress the common mode signal by the circuit of FIG. 4 means a reduction in current ' i_{12} ' expressed by the equation (7). According to the equation (7), the current ' i_{12} ' is reduced if the denominator of the right side of the equation (7) increases. Consideration will now be given to the denominator ($Z_1 \cdot Z_2 + \omega^2 \cdot M^2$) of the right side of the equation (7).

[0052] First, since Z_1 is expressed by the equation (2), Z_1 increases as the inductance L_{11} of the third winding 13 increases, and Z_1 increases as the capacitance C_{11} of the capacitor 51 increases.

[0053] Next, since Z_2 is expressed by the equation (3), Z_2 increases as the inductance L_{12} of the first winding 11 increases. Therefore, the current ' i_{12} ' is reduced if the inductance L_{12} is increased.

[0054] Since the denominator of the right side of the equation (7) includes $\omega^2 \cdot M^2$, the current ' i_{12} ' is reduced by increasing the mutual inductance M . As shown in the equation (1), the coupling coefficient K is proportional to the mutual inductance M . Therefore, if the coupling coefficient K is increased, the effect of suppressing common mode signals by the circuit of FIG. 4 is enhanced. Since the mutual inductance M is included in a form of square in the denominator of the right side of the equation (7), the effect of suppressing common mode signals greatly varies, depending on the value of coupling coefficient K .

[0055] The foregoing description similarly applies to a portion of the common mode signal suppressing circuit of FIG. 2 that relates to suppression of signals passing through the conductor line 4.

[0056] If the common mode signal source is located closer to the first and second points A and B than the third and fourth points C and D, the roles of the third winding 13 and the phase-inverted signal transmitting circuit 15 are the reverse of the roles described with reference to FIG. 3 and FIG. 4. However, the foregoing description similarly applies to such a case, too.

[0057] According to the embodiment as thus described, it is possible to implement the common mode signal suppressing circuit capable of effectively suppressing common mode signals in a wide frequency range and achieving a reduction in size.

[0058] According to the embodiment, it is possible to implement the common mode signal suppressing circuit that has a greater effect of suppressing common mode signals although it has a smaller number of components than a conventional EMI filter does and is inexpensive.

[0059] According to the embodiment, if the phase-inverted signal transmitting circuit 15 is made up of the capacitors 51 and 52, it is possible only by the capacitors 51 and 52 to perform detection of common mode signals and generation of phase-inverted signals each having a phase opposite to the phase of each of the common

mode signals detected. As a result, the number of components is further reduced in this case.

[0060] The common mode signal suppressing circuit of the embodiment may be used as a means for reducing a ripple voltage and noise developed by a power transformer circuit, or a means for avoiding communications signals on an indoor power line from leaking to an outdoor power line.

[Second Embodiment]

[0061] FIG. 5 is a schematic diagram illustrating a basic configuration of a common mode signal suppressing circuit of a second embodiment of the invention. The common mode signal suppressing circuit of the second embodiment has a configuration of the common mode signal suppressing circuit of the first embodiment to which an impedance element 16 is added. The impedance element 16 is provided at points on the conductor lines 3 and 4 between the first point A and the third point C and between the second point B and the fourth point D. The impedance element 16 reduces the peak value of a common mode signal passing therethrough. As a result, in the common mode signal suppressing circuit of the second embodiment, the difference between the peak value of the common mode signal propagating via the impedance element 16 and the peak value of the phase-inverted signal injected to the conductor lines 3 and 4 via the phase-inverted signal transmitting circuit 15 is reduced. As a result, according to the common mode signal suppressing circuit of the embodiment, it is possible to suppress common mode signals in a wider frequency range more effectively.

[0062] FIG. 6 is a schematic diagram illustrating a specific example of configuration of the common mode signal suppressing circuit of FIG. 5. In this example, as in the example illustrated in FIG. 2, the phase-inverted signal transmitting circuit 15 is made up of the high-pass filter 15A. The high-pass filter 15A includes the capacitors 51 and 52.

[0063] In the example of FIG. 6, the impedance element 16 incorporates: a fourth winding 61 inserted to the conductor line 3; and a fifth winding 62 that is inserted to the conductor line 4 and coupled to the fourth winding 61 through a magnetic core 60 and that suppresses common mode signals in cooperation with the fourth winding 61. For example, the numbers of windings 61 and 62 may be equal. The core 60 and the windings 61 and 62 make up a common mode choke coil. That is, the windings 61 and 62 are wound around the core 60 in such directions that, when magnetic fluxes are induced in the core 60 by currents flowing through the windings 61 and 62 when a normal mode current is fed to the windings 61 and 62, these fluxes are cancelled out by each other. The windings 61 and 62 thereby suppress common mode signals and allow normal mode signals to pass.

[0064] Reference is now made to FIG. 7 to describe

details of the operation of the common mode signal suppressing circuit of the second embodiment. FIG. 7 illustrates a portion of the common mode signal suppressing circuit of FIG. 6 that relates to suppression of signals passing through the conductor line 3. The circuit of FIG. 7 incorporates the terminals 1a and 2a, the first winding 11, the third winding 13, the capacitor 51 and the fourth winding 61. The common mode signal source 21 and the load 22 are connected to the circuit of FIG. 7. The common mode signal source 21 is connected between the terminal 1a and the ground GND, and creates a potential difference V_{in1} between the terminal 1a and the ground GND. The load 22 is connected between the terminal 2a and the ground GND, and has an impedance Z_{o1} .

[0065] In the circuit of FIG. 7, the inductance of the third winding 13 is L_{11} , the inductance of the first winding 11 is L_{12} , the capacitance of the capacitor 51 is C_{11} , and the inductance of the fourth winding 61 is L_{21} . The current passing through the capacitor 51 and the third winding 13 is ' i_{11} ', and the sum of impedances on the path of the current i_{11} is Z_1 . The current passing through the fourth winding 61 and the first winding 11 is ' i_{12} ', and the sum of impedances on the path of the current i_{12} is Z_2 . The mutual inductance between the first winding 11 and the third winding 13 is M , and the coupling coefficient between the first winding 11 and the third winding 13 is K . The coupling coefficient K is expressed by the above-mentioned equation (1).

[0066] In the second embodiment, the sum of impedances Z_1 is expressed by the above-mentioned equation (2), and the sum of impedances Z_2 is expressed by the following equation (8).

$$Z_2 = Z_{o1} + j\omega(L_{12} + L_{21}) \quad (8)$$

[0067] The potential difference V_{in1} is expressed by the above-mentioned equations (4) and (5). In the second embodiment, the equation that expresses the current ' i_{12} ' without including the current ' i_{11} ' is the above-mentioned equation (7), as in the first embodiment.

[0068] To suppress the common mode signal by the circuit of FIG. 7 means a reduction in current ' i_{12} ' expressed by the equation (7). According to the equation (7), the current ' i_{12} ' is reduced if the denominator of the right side of the equation (7) increases. Consideration will now be given to the denominator ($Z_1 \cdot Z_2 + \omega^2 \cdot M^2$) of the right side of the equation (7).

[0069] First, since Z_1 is expressed by the equation (2), Z_1 increases as the inductance L_{11} of the third winding 13 increases, and Z_1 increases as the capacitance C_{11} of the capacitor 51 increases. This is the same as described in the first embodiment.

[0070] Next, in the circuit of FIG. 7, since Z_2 is expressed by the equation (8), Z_2 increases as the sum of the inductance L_{12} of the first winding 11 and the inductance L_{21} of the fourth winding 61 increases. There-

fore, the current 'i12' is reduced if at least one of the inductance L12 and the inductance L21 is increased. In addition, the equation (7) shows that, although it is possible to suppress common mode signals only by the first winding 11, it is possible to suppress common mode signals more effectively by adding the fourth winding 61.

[0071] As in the first embodiment, the current 'i12' is reduced by increasing the mutual inductance M.

[0072] The foregoing description similarly applies to a portion of the common mode signal suppressing circuit of FIG. 6 that relates to suppression of signals passing through the conductor line 4.

[0073] If the common mode signal source is located closer to the first and second points A and B than the third and fourth points C and D, the roles of the third winding 13 and the phase-inverted signal transmitting circuit 15 are the reverse of the roles described with reference to FIG. 7. However, the foregoing description similarly applies to such a case, too.

[0074] Reference is now made to FIG. 8 to describe the result of determining the relationship between the effect of suppressing common mode signals and the inductances of the windings 61 and 62 of the common mode signal suppressing circuit of FIG. 6 by simulation. FIG. 8 shows frequency characteristics of gains obtained by simulation for a reference circuit and the common mode signal suppressing circuit of FIG. 6.

[0075] The reference circuit comprises: a pair of terminals 1a and 1b; another pair of terminals 2a and 2b; a first inductance element having an end connected to the terminal 1a and the other end connected to the terminal 2a; and a second inductance element having an end connected to the terminal 1b and the other end connected to the terminal 2b. A line of FIG. 8 indicated with numeral 31 shows the characteristic of the reference circuit when the inductance of each of the above-mentioned first and second inductance elements is 33 μ H. A line of FIG. 8 indicated with numeral 32 shows the characteristic of the reference circuit when the inductance of each of the first and second inductance elements is 90 μ H.

[0076] Lines of FIG. 8 indicated with numerals 33 to 38 show the characteristics of the common mode signal suppressing circuit of FIG. 6. In the simulation, the capacitance of each of the capacitors 51 and 52 is 1000 pF, the inductance of each of the first winding 11, the second winding 12 and the third winding 13 is 30 μ H, and the coupling coefficient between the winding 13 and the windings 11 and 12 is 0.995. The value of 0.995 is a value that can be obtained as the coupling coefficient.

[0077] In the simulation no difference in characteristic of the common mode signal suppressing circuit is observed between the case in which the common mode signal source is located at a point closer to the first and second points A and B and the case in which the common mode signal source is located at a point closer to the third and fourth points C and D.

[0078] The line indicated with numeral 33 shows the

characteristic obtained when the inductance of each of the windings 61 and 62 is zero. The configuration of the common mode signal suppressing circuit of FIG. 6 in this case is the same as the configuration of the common mode signal suppressing circuit of FIG. 2. The line indicated with numeral 34 shows the characteristic obtained when the inductance of each of the windings 61 and 62 is 0.3 μ H. The line indicated with numeral 35 shows the characteristic obtained when the inductance of each of the windings 61 and 62 is 3 μ H.

The line indicated with numeral 36 shows the characteristic obtained when the inductance of each of the windings 61 and 62 is 30 μ H. The line indicated with numeral 37 shows the characteristic obtained when the inductance of each of the windings 61 and 62 is 60 μ H. The line indicated with numeral 38 shows the characteristic obtained when the inductance of each of the windings 61 and 62 is 600 μ H.

[0079] The result of the simulation shown in FIG. 8 will now be considered. First, the following facts will be obtained from the comparison among the lines indicated with numerals 31, 32 and 35. The common mode signal suppressing circuit wherein the inductance of the first winding 11 is 30 μ H, the inductance of the fourth winding 61 is 3 μ H, and the sum of these inductances is 33 μ H has a greater effect of suppressing common mode signals in a frequency range of approximately 1 MHz and higher, compared with the reference circuit wherein the inductance of the inductance element is 33 μ H. This common mode signal suppressing circuit has a greater effect of suppressing common mode signals in a frequency range of approximately 3 MHz and higher, compared with the reference circuit wherein the inductance of the inductance element is 90 μ H. Because of this feature, according to the embodiment, it is possible to make the inductance element smaller, compared with the reference circuit, and it is thereby possible to reduce the entire circuit in size.

[0080] The result of the simulation shown in FIG. 8 will now be considered. First, the following facts will be obtained from the comparison among the lines indicated with numerals 31, 32 and 35. The common mode signal suppressing circuit wherein the inductance of the first winding 11 is 30 μ H, the inductance of the fourth winding 61 is 3 μ H, and the sum of these inductances is 33 μ H has a greater effect of suppressing common mode signals in a frequency range of approximately 1 MHz and higher, compared with the reference circuit wherein the inductance of the inductance element is 33 μ H. This common mode signal suppressing circuit has a greater effect of suppressing common mode signals in a frequency range of approximately 3 MHz and higher, compared with the reference circuit wherein the inductance of the inductance element is 90 μ H. Because of this feature, according to the embodiment, it is possible to make the inductance element smaller, compared with the reference circuit, and it is thereby possible to reduce the entire circuit in size.

[0081] If the line with numeral 31 and the line with numeral 33 are compared, it is noted that the effect of suppressing common mode signals is obtained even when the inductance of the windings 61 and 62 is zero, that is, when the impedance element 16 is not provided.

[0082] However, as the comparison among the lines with numerals 33 to 38 shows, a greater effect of suppressing common mode signals is obtained when the impedance element 16 is provided, compared with the case in which the impedance element 16 is not provided. Moreover, the effect of suppressing common mode signals increases as the inductance of the windings 61 and 62 increases. However, the impedance element 16 is increased in dimensions as the inductance of the windings 61 and 62 increases. Therefore, if the inductance of the windings 61 and 62 exceeds 600 μH , the practicality is reduced. It is noted that, if the inductance of the windings 11 to 13 is 30 μH , a sufficient effect of suppressing common mode signals is obtained as long as the inductance of the windings 61 and 62 is 30 or 60 μH . These findings indicate that it is sufficient that the inductance of the windings 61 and 62 is 30 or 60 μH . In addition, it would be preferred that the inductance of the windings 61 and 62 is of a value similar to that of the windings 11 to 13.

[0083] The consideration of FIG. 8 indicates that the inductance of the windings 61 and 62 should preferably fall within a range of 0.3 μH to 600 μH inclusive, more preferably within a range of 3 μH to 60 μH inclusive, and still more preferably within a range of 3 μH to 30 μH inclusive.

[0084] Reference is now made to FIG. 9 to describe the result of determining the relationship between the effect of suppressing common mode signals and the coupling coefficient between the winding 13 and the windings 11 and 12 of the common mode signal suppressing circuit of FIG. 6 by simulation. FIG. 9 shows frequency characteristics of gains obtained by simulation for the above-mentioned reference circuit and the common mode signal suppressing circuit of FIG. 6.

[0085] Lines of FIG. 9 indicated with numerals 41 and 42 show the characteristics of the reference circuit under the conditions the same as those in the cases for the lines of FIG. 8 indicated with numerals 31 and 32.

[0086] Lines of FIG. 9 indicated with numerals 43 to 46 show the characteristics of the common mode signal suppressing circuit of FIG. 6. In the simulation, the capacitance of the capacitors 51 and 52 is 1000 pF, and the inductance of each of the windings 11, 12, 13, 61 and 62 is 30 μH . The lines with numerals 43 to 46 show the characteristics obtained in the cases in which the coupling coefficients between the winding 13 and the windings 11 and 12 are 0.7, 0.9, 0.995, and 1, respectively.

[0087] Consideration will now be given to the result of the simulation shown in FIG. 9. First, in the common mode signal suppressing circuit, if the coupling coefficient is 0.7 or greater, a greater effect of suppressing

common mode signals is obtained, compared with the reference circuit. As the coupling coefficient increases, the effect of suppressing common mode signals is enhanced. FIG. 9 being considered, the coupling coefficient should preferably be 0.7 or greater, and more preferably be 0.9 or greater, and still more preferably be 0.995 or greater.

[0088] According to the common mode signal suppressing circuit of the embodiment as thus described, it is possible to suppress common mode signals in a wider frequency range more effectively, compared with the common mode signal suppressing circuit of the first embodiment.

[0089] The remainder of configuration, operations and effects of the second embodiment are similar to those of the first embodiment.

[Third Embodiment]

[0090] FIG. 10 is a schematic diagram illustrating a basic configuration of a normal mode signal suppressing circuit of a third embodiment of the invention. The normal mode signal suppressing circuit of the third embodiment comprises a pair of terminals 101a and 101b, another pair of terminals 102a and 102b, a conductor line 103 connecting the terminals 101a and 102a to each other, and a conductor line 104 connecting the terminals 101b and 102b to each other. The normal mode signal suppressing circuit is designed to be connected to a power line for transmitting alternating current power or direct current power. The power line includes two power conductor lines. The normal mode signal suppressing circuit is designed to be inserted somewhere along the two power conductor lines. The terminals 101a and 102a are connected to one of the power conductor lines while the terminals 101b and 102b are connected to the other of the power conductor lines. A source of normal mode signals to be suppressed by the normal mode signal suppressing circuit is connected to the terminals 101a and 101b or the terminals 102a and 102b. Therefore, the normal mode signals to be suppressed are inputted to the normal mode signal suppressing circuit from the terminals 101a and 101b or the terminals 102a and 102b.

[0091] Here, the normal mode signals are signals transmitted by the two power conductor lines and creating a potential difference between the two power conductor lines. The normal mode signals to be suppressed include noise and unwanted communications signals.

[0092] The normal mode signal suppressing circuit further comprises: a first inductance element 111 inserted to the conductor line 103 at a specific first point E; and a second inductance element 112 coupled to the first inductance element 111 through a magnetic core 113 such that a mutual inductance is generated between the second inductance element 112 and the first inductance element 111. The inductance elements 111 and 112 have windings, and the turns ratio of the windings

may be 1: 1, for example.

[0093] The normal mode signal suppressing circuit further comprises a phase-inverted signal transmitting circuit 115 connected to the second inductance element 112 and to the conductor line 103 at a point F different from the first point E. The phase-inverted signal transmitting circuit 115 transmits phase-inverted signals for suppressing normal mode signals. The phase-inverted signal transmitting circuit 115 has an end connected to the conductor line 103 at the point F. The circuit 115 has the other end connected to an end of the second inductance element 112. The other end of the second inductance element 112 is connected to the conductor line 104. The phase-inverted signal transmitting circuit 115 corresponds to the phase-inverted signal transmitting means of the invention.

[0094] The normal mode signal suppressing circuit further comprises an impedance element 116 that is provided at a point on the conductor line 103 between the first point E and the second point F and that reduces the peak value of a normal mode signal passing therethrough.

[0095] FIG. 11 is a schematic diagram illustrating a specific example of configuration of the normal mode signal suppressing circuit of FIG. 10. In this example, the phase-inverted signal transmitting circuit 115 is made up of a high-pass filter 115A for allowing signals having a specific frequency or higher to pass among normal mode signals or phase-inverted signals. The high-pass filter 115A includes a capacitor 115a. The capacitor 115a has an end connected to the conductor line 103 at the point F. The capacitor 115a has the other end connected to an end of the second inductance element 112.

[0096] In the example shown in FIG. 11, the impedance element 116 is made up of a third inductance element 116A. The third inductance element 116A has an end connected to the terminal 101a and the other end connected to an end of the first inductance element 111.

[0097] The operation of the normal mode signal suppressing circuit of the embodiment will now be described. First, the operation of the normal mode signal suppressing circuit will be described, wherein the normal mode signal source is located at a point closer to the second point F than the first point E except a point between the first point E and the second point F. In this case, the phase-inverted signal transmitting circuit 115 detects a normal mode signal on the conductor line 103 at the second point F, and supplies a phase-inverted signal to the second inductance element 112, the phase-inverted signal having a phase opposite to the phase of the normal mode signal detected. The second inductance element 112 injects the phase-inverted signal to the conductor line 103 at the first point E through the first inductance element 111. As a result, the normal mode signal is suppressed on a portion of the conductor line 103 from the first point E onward along the direction of travel of the normal mode signal.

[0098] Next, the operation of the normal mode signal suppressing circuit will be described, wherein the normal mode signal source is located at a point closer to the first point E than the second point F except a point between the first point E and the second point F. In this case, the second inductance element 112 detects a normal mode signal on the conductor line 103 at the first point E. The phase-inverted signal transmitting circuit 115 injects a phase-inverted signal to the conductor line 103 at the second point F, the phase-inverted signal having a phase opposite to the phase of the normal mode signal detected by the second inductance element 112. As a result, the normal mode signal is suppressed on a portion of the conductor line 103 from the second point F onward along the direction of travel of the normal mode signal.

[0099] According to the embodiment, the impedance element 116 reduces the peak value of a signal passing therethrough. As a result, the difference between the peak value of the normal mode signal propagating via the impedance element 116 and the peak value of the phase-inverted signal injected to the conductor line 103 via the phase-inverted signal transmitting circuit 115 is reduced.

[0100] Reference is now made to FIG. 12 to describe the principle of suppression of normal mode signals by the normal mode signal suppressing circuit of the embodiment. Here, a case will be described wherein the normal mode signal source is located at a point closer to the second point F than the first point E. FIG. 12 illustrates the configuration of FIG. 11 from which the third inductance element 116A is removed. In the following description, it is assumed that the impedance of the high-pass filter 115A (the capacitor 115a) is zero, the turns ratio between the first inductance element 111 and the second inductance element 112 is 1: 1, for example, and the coupling coefficient between the first inductance element 111 and the second inductance element 112 is 1.

[0101] It is assumed that, in the circuit of FIG. 12, a normal mode signal that creates a potential difference V_{in2} between the terminals 101a and 101b is inputted to the terminals 101a and 101b. If the normal mode signal has a frequency within the pass band of the high-pass filter 115A, the normal mode signal passes through the high-pass filter 115A, and a phase shift of 180 degrees occurs at the same time by means of the operation of the capacitor 115a. As a result, a potential difference $-V_{in2}$ is created between the ends of the second inductance element 112. A potential difference $-V_{in2}$ is also created between the ends of the first inductance element 111 in accordance with the potential difference $-V_{in2}$ created between the ends of the second inductance element 112. This is expressed by the equation below where the potential difference between the terminals 102a and 102b is V_{o2} .

$$V_{o2} = V_{in2} + (-V_{in2}) = 0$$

[0102] According to the circuit of FIG. 12 as thus described, as long as the impedance of the high-pass filter 115A is zero and the coupling coefficient between the first inductance element 111 and the second inductance element 112 is 1, it is possible to completely remove normal mode signals at any frequency within the pass band of the high-pass filter 115A.

[0103] In practice, however, it is impossible that the impedance of the high-pass filter 115A is zero, and the impedance varies in response to the frequency. In particular, if the high-pass filter 115A is made up of the capacitor 115a, a series resonant circuit is made up of the capacitor 115a and the second inductance element 112. Therefore, the impedance of the signal path including the capacitor 115a and the second inductance element 112 is reduced only in a narrow frequency range around the resonant frequency of the series resonant circuit. As a result, the circuit of FIG. 12 is capable of removing normal mode signals only in a narrow frequency range.

[0104] In addition, the coupling coefficient between the first inductance element 111 and the second inductance element 112 is smaller than 1 in practice. Therefore, it is impossible that voltage of a value the same as that of the voltage supplied to the second inductance element 112 is generated at the first inductance element 111.

[0105] Because of the foregoing reasons, the circuit of FIG. 12 is not capable of effectively suppressing normal mode signals in a wide frequency range.

[0106] According to the normal mode signal suppressing circuit of the embodiment, the impedance element 116 is provided on the conductor line 103 between the first point E and the second point F so as to reduce the peak value of a normal mode signal passing there-through. As a result, in the normal mode signal suppressing circuit, the difference between the peak value of the normal mode signal propagating via the impedance element 116 and the peak value of the phase-inverted signal injected to the conductor line 103 via the phase-inverted signal transmitting circuit 115 is reduced. As a result, according to the normal mode signal suppressing circuit, it is possible to effectively suppress normal mode signals in a wide frequency range.

[0107] Reference is now made to FIG. 13 to describe details of the operation of the normal mode signal suppressing circuit of the embodiment. FIG. 13 illustrates a circuit in which a normal mode signal source 121 and a load 122 are connected to the normal mode signal suppressing circuit of FIG. 11. The normal mode signal source 121 is connected between the terminals 101a and 101b, and creates a potential difference V_{in2} between the terminals 101a and 101b. The load 122 is connected between the terminals 102a and 102b, and has an impedance Z_{o2} .

[0108] In the circuit of FIG. 13, the inductance of the

second inductance element 112 is L_{31} , the inductance of the first inductance element 111 is L_{32} , the capacitance of the capacitor 115a is C_{21} , and the inductance of the third inductance element 116A is L_{41} . The current passing through the capacitor 115a and the second inductance element 112 is ' i_{21} ', and the sum of impedances on the path of the current i_{21} is Z_3 . The current passing through the third inductance element 116A and the first inductance element 111 is ' i_{22} ', and the sum of impedances on the path of the current i_{22} is Z_4 .

[0109] The mutual inductance between the first inductance element 111 and the second inductance element 112 is M , and the coupling coefficient between the first inductance element 111 and the second inductance element 112 is K . The coupling coefficient K is expressed by the following equation (9).

$$K = M / \sqrt{L_{31} \cdot L_{32}} \quad (9)$$

[0110] The above-mentioned sums Z_3 and Z_4 of impedances are expressed by the following equations (10) and (11), respectively, where ' j ' indicates $\sqrt{-1}$, and ' ω ' indicates the angular frequency of the normal mode signal.

$$Z_3 = j(\omega L_{31} - 1/\omega C_{21}) \quad (10)$$

$$Z_4 = Z_{o2} + j\omega(L_{32} + L_{41}) \quad (11)$$

[0111] The potential difference V_{in2} is expressed by the following equations (12) and (13).

$$V_{in2} = Z_3 \cdot i_{21} + j\omega M \cdot i_{22} \quad (12)$$

$$V_{in2} = Z_4 \cdot i_{22} + j\omega M \cdot i_{21} \quad (13)$$

[0112] Based on the equations (10) to (13), an equation that expresses the current ' i_{22} ' without including the current ' i_{21} ' will be obtained below. First, the following equation (14) is obtained from the equation (12).

$$i_{21} = (V_{in2} - j\omega M \cdot i_{22}) / Z_3 \quad (14)$$

[0113] Next, the equation (14) is substituted into the equation (13), and the following equation (15) is thereby obtained.

$$i_{22} = V_{in2}(Z_3 - j\omega M) / (Z_3 \cdot Z_4 + \omega^2 \cdot M^2) \quad (15)$$

[0114] To suppress the normal mode signal by the

normal mode signal suppressing circuit of FIG. 13 means a reduction in current 'i22' expressed by the equation (15). According to the equation (15), the current 'i22' is reduced if the denominator of the right side of the equation (15) increases. Consideration will now be given to the denominator ($Z3 - Z4 + \omega^2 \cdot M^2$) of the right side of the equation (15).

[0115] First, since Z3 is expressed by the equation (10), Z3 increases as the inductance L31 of the second inductance element 112 increases, and Z3 increases as the capacitance C21 of the capacitor 115a increases.

[0116] Next, since Z4 is expressed by the equation (11), Z4 increases as the sum of the inductance L32 of the first inductance element 111 and the inductance L41 of the third inductance element 116A increases. Therefore, the current 'i22' is reduced if at least one of the inductance L32 and the inductance L41 is increased. The equation (15) indicates that, although it is possible to suppress normal mode signals only by the first inductance element 111, it is possible to suppress normal mode signals more effectively if the third inductance element 116A is added.

[0117] Since the denominator of the right side of the equation (15) includes $\omega^2 \cdot M^2$, the current 'i22' is reduced by increasing the mutual inductance M. As shown in the equation (9), the coupling coefficient K is proportional to the mutual inductance M. Therefore, if the coupling coefficient K is increased, the effect of suppressing normal mode signals by the normal mode signal suppressing circuit of FIG. 13 is enhanced. Since the mutual inductance M is included in a form of square in the denominator of the right side of the equation (15), the effect of suppressing normal mode signals greatly varies, depending on the value of coupling coefficient K.

[0118] If the normal mode signal source is located closer to the first point E than the second point F, the roles of the second inductance element 112 and the phase-inverted signal transmitting circuit 115 are the reverse of the roles described with reference to FIG. 12 and FIG. 13. However, the foregoing description similarly applies to such a case, too.

[0119] Reference is now made to FIG. 14 to describe the result of determining the relationship between the effect of suppressing normal mode signals and the inductance of the third inductance element 116A of the normal mode signal suppressing circuit of FIG. 11 by simulation. FIG. 14 shows frequency characteristics of gains obtained by simulation for a reference circuit and the normal mode signal suppressing circuit of FIG. 11.

[0120] The reference circuit comprises: a pair of terminals 101a and 101b; another pair of terminals 102a and 102b; and an inductance element having an end connected to the terminal 101a and the other end connected to the terminal 102a. A line of FIG. 14 indicated with numeral 131 shows the characteristic of the reference circuit when the inductance of the above-mentioned inductance element is 33 μH . A line of FIG. 14 indicated with numeral 132 shows the characteristic of

the reference circuit when the inductance of the inductance element is 90 μH .

[0121] Lines of FIG. 14 indicated with numerals 133 to 138 show the characteristics of the normal mode signal suppressing circuit of FIG. 11. In the simulation, the capacitance of the capacitor 115a is 0.01 μF , the inductance of each of the first inductance element 111 and the second inductance element 112 is 30 μH , and the coupling coefficient between the first inductance element 111 and the second inductance element 112 is 0.995. The value of 0.995 is a value that can be obtained as the coupling coefficient.

[0122] In the simulation no difference in characteristic of the normal mode signal suppressing circuit is observed between the case in which the normal mode signal source is located at a point closer to the first point E and the case in which the normal mode signal source is located at a point closer to the second point F.

[0123] The line indicated with numeral 133 shows the characteristic obtained when the inductance of the third inductance element 116A is zero. The configuration of the normal mode signal suppressing circuit of FIG. 11 in this case is the same as the configuration of the circuit of FIG. 12. The line indicated with numeral 134 shows the characteristic obtained when the inductance of the third inductance element 116A is 0.3 μH . The line indicated with numeral 135 shows the characteristic obtained when the inductance of the third inductance element 116A is 3 μH . The line indicated with numeral 136 shows the characteristic obtained when the inductance of the third inductance element 116A is 30 μH . The line indicated with numeral 137 shows the characteristic obtained when the inductance of the third inductance element 116A is 60 μH . The line indicated with numeral 138 shows the characteristic obtained when the inductance of the third inductance element 116A is 600 μH .

[0124] The result of the simulation shown in FIG. 14 will now be considered. First, the following facts will be obtained from the comparison between the lines indicated with numerals 132 and 135. The normal mode signal suppressing circuit wherein the inductance of the first inductance element 111 is 30 μH , the inductance of the third inductance element 116A is 3 μH , and the sum of these inductances is 33 μH has a greater effect of suppressing normal mode signals in a frequency range of 1 MHz and higher, compared with the reference circuit wherein the inductance of the inductance element is 90 μH . Because of this feature, according to the embodiment, it is possible to make the inductance element smaller, compared with the reference circuit, and it is thereby possible to reduce the entire circuit in size.

[0125] If the lines with numerals 133 to 138 are compared, it is noted that a greater effect of suppressing normal mode signals is obtained as the inductance of the third inductance element 116A increases. However, the third inductance element 116A is increased in dimensions as the inductance of the third inductance element 116A increases. Therefore, if the inductance of the third

inductance element 116A exceeds 600 μH , the practicality is reduced. It is noted that, when the inductance of the first inductance element 111 is 30 μH , a sufficient effect of suppressing normal mode signals is obtained as long as the inductance of the third inductance element 116A is 30 or 60 μH . These findings indicate that it is sufficient that the inductance of the third inductance element 116A is 30 or 60 μH . In addition, it is preferred that the inductance of the third inductance element 116A is of a value similar to that of the first inductance element 111.

[0126] As the comparison between the lines with numerals 131 and 134 indicates, it is possible to obtain the effect of suppressing normal mode signals even if the inductance of the third inductance element 116A is around 0.3 μH .

[0127] The consideration of FIG. 14 indicates that the inductance of the third inductance element 116A should preferably fall within a range of 0.3 μH to 600 μH inclusive, more preferably within a range of 3 μH to 60 μH inclusive, and still more preferably within a range of 3 μH to 30 μH inclusive.

[0128] Reference is now made to FIG. 15 to describe the result of determining the relationship between the effect of suppressing normal mode signals and the coupling coefficient between first inductance element 111 and the second inductance element 112 of the normal mode signal suppressing circuit of FIG. 11 by simulation. FIG. 15 shows frequency characteristics of gains obtained by simulation for the above-mentioned reference circuit and the normal mode signal suppressing circuit of FIG. 11.

[0129] Lines of FIG. 15 indicated with numerals 141 and 142 show the characteristics of the reference circuit under the conditions the same as those in the cases for the lines of FIG. 14 indicated with numerals 131 and 132.

[0130] Lines of FIG. 15 indicated with numerals 143 to 146 show the characteristics of the normal mode signal suppressing circuit of FIG. 11. In the simulation, the capacitance of the capacitor 115a is 0.01 μF , and the inductance of each of the first inductance element 111, the second inductance element 112 and the third inductance element 116A is 30 μH . The lines with numerals 143 to 146 show the characteristics obtained in the cases in which the coupling coefficients between the first inductance element 111 and the second inductance element 112 are 0.7, 0.9, 0.995, and 1, respectively.

[0131] Consideration will now be given to the result of the simulation shown in FIG. 15. First, in the normal mode signal suppressing circuit, if the coupling coefficient is 0.7 or greater, a greater effect of suppressing normal mode signals is obtained, compared with the reference circuit. As the coupling coefficient increases, the effect of suppressing normal mode signals is enhanced. FIG. 15 being considered, the coupling coefficient should preferably be 0.7 or greater, and more preferably be 0.9 or greater, and still more preferably be 0.995 or

greater.

[0132] According to the embodiment as thus described, it is possible to implement the normal mode signal suppressing circuit capable of suppressing normal mode signals in a wide frequency range effectively, and achieving a reduction in size.

[0133] According to the embodiment, it is possible to implement the normal mode signal suppressing circuit that has a greater effect of suppressing normal mode signals although it has a smaller number of components than the conventional EMI filter does and is inexpensive.

[0134] According to the embodiment, if the phase-inverted signal transmitting circuit 115 is made up of the capacitor 115a, it is possible only by the capacitor 115a to perform detection of normal mode signals and generation of a phase-inverted signal having a phase opposite to that of the normal mode signal detected. As a result, the number of components is further reduced in this case.

[0135] The normal mode signal suppressing circuit of the embodiment may be used as a means for reducing a ripple voltage and noise developed by a power transformer circuit, or a means for avoiding communications signals on an indoor power line from leaking to an outdoor power line.

[Fourth Embodiment]

[0136] FIG. 16 is a schematic diagram illustrating the configuration of a normal mode signal suppressing circuit of a fourth embodiment of the invention. The basic configuration of the normal mode signal suppressing circuit of the fourth embodiment is the same as that of the third embodiment. A difference between the fourth and third embodiments is that the high-pass filter 115A as the phase-inverted signal transmitting circuit 115 of the fourth embodiment incorporates a plurality of capacitors 151, 152, ... that are combined. It is acceptable that the number of capacitors incorporated in the high-pass filter 115A is two or greater.

[0137] Each of the capacitors 151, 152, ... has an end connected to the conductor line 103 at the second point F, and the other end connected to an end of the second inductance element 112. Therefore, the capacitors 151, 152, ... are connected to one another in parallel. The capacitors 151, 152, ... have different capacitances. The high-pass filter 115A incorporating such capacitors 151, 152, ... makes it possible that the high-pass filter 115A is designed to have a desired frequency characteristic. For example, according to the high-pass filter 115A of the fourth embodiment, it is possible to design the frequency characteristic of the high-pass filter 115A such that the pass band is wider than that of the high-pass filter 115A of the third embodiment.

[0138] The remainder of configuration, operations and effects of the fourth embodiment are similar to those of the third embodiment.

[0139] The present invention is not limited to the fore-

going embodiments but may be practiced in still other ways. For example, each of the phase-inverted signal transmitting circuits 15 and 115 is not limited to a high-pass filter but may be a band-pass filter.

[0140] As thus described, according to the common mode signal suppressing circuit of the invention, it is possible to implement the common mode signal suppressing circuit capable of effectively suppressing common mode signals in a wide frequency range and achieving a reduction in size.

[0141] According to the normal mode signal suppressing circuit of the invention, it is possible to implement the normal mode signal suppressing circuit capable of effectively suppressing normal mode signals in a wide frequency range and achieving a reduction in size.

[0142] Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may be practiced otherwise than as specifically described.

Claims

1. A common mode signal suppressing circuit for suppressing common mode signals propagating with identical phases through two conductor lines, the common mode signal suppressing circuit comprising:

a first winding inserted to one of the conductor lines at a specific first point;

a second winding that is inserted to the other of the conductor lines at a second point corresponding to the first point and is coupled to the first winding, the second winding suppressing the common mode signals in cooperation with the first winding;

a third winding coupled to the first and second windings such that a mutual inductance is generated between the third winding and the first and second windings; and

a phase-inverted signal transmitting means connected to the third winding and to the one of the conductor lines at a third point different from the first point, the transmitting means being further connected to the other of the conductor lines at a fourth point corresponding to the third point and different from the second point, the transmitting means transmitting a phase-inverted signal for suppressing the common mode signals, wherein:

when a source of the common mode signals is located at a point closer to the third and fourth points than the first and second points except a point between the first and

third points and a point between the second and fourth points, the transmitting means detects a common mode signal and supplies the phase-inverted signal to the third winding, the phase-inverted signal having a phase opposite to a phase of the common mode signal detected, and the third winding injects the phase-inverted signal to the two conductor lines through the first and second windings; and when the source of the common mode signals is located at a point closer to the first and second points than the third and fourth points except a point between the first and third points and a point between the second and fourth points, the third winding detects a common mode signal, and the transmitting means injects the phase-inverted signal to the two conductor lines, the phase-inverted signal having a phase opposite to a phase of the common mode signal detected by the third winding.

2. The common mode signal suppressing circuit according to claim 1, further comprising an impedance element provided on the two conductor lines at a point between the first and third points and a point between the second and fourth points, the impedance element reducing a peak value of a common mode signal passing therethrough.
3. The common mode signal suppressing circuit according to claim 1, wherein the phase-inverted signal transmitting means incorporates a high-pass filter for allowing a common mode signal to pass therethrough.
4. The common mode signal suppressing circuit according to claim 3, wherein the high-pass filter incorporates a capacitor.
5. The common mode signal suppressing circuit according to claim 1, wherein the impedance element incorporates: a fourth winding inserted to one of the conductor lines; and a fifth winding that is inserted to the other of the conductor lines and coupled to the fourth winding and that suppresses the common mode signals in cooperation with the fourth winding.
6. The common mode signal suppressing circuit according to claim 5, wherein each of the fourth and fifth windings has an inductance of 0.3 μ H or greater.
7. The common mode signal suppressing circuit according to claim 1, wherein a coupling coefficient between the third winding and the first and second windings is 0.7 or greater.

8. A normal mode signal suppressing circuit for suppressing normal mode signals transmitted by two conductor lines and creating a potential difference between the two conductor lines, the normal mode signal suppressing circuit comprising:

a first inductance element inserted to one of the conductor lines at a specific first point;
 a second inductance element coupled to the first inductance element such that a mutual inductance is generated between the first and second inductance elements;
 a phase-inverted signal transmitting means connected to the second inductance element and to the one of the conductor lines at a second point different from the first point, the transmitting means transmitting a phase-inverted signal for suppressing the normal mode signals; and
 an impedance element provided on the one of the conductor lines at a point between the first and second points, the impedance element reducing a peak value of a normal mode signal passing therethrough, wherein:

when a source of the normal mode signals is located at a point closer to the second point than the first point except a point between the first and second points, the transmitting means detects a normal mode signal and supplies the phase-inverted signal to the second inductance element, the phase-inverted signal having a phase opposite to a phase of the normal mode signal detected, and the second inductance element injects the phase-inverted signal to the one of the conductor lines through the first inductance element; and
 when the source of the normal mode signals is located at a point closer to the first point than the second point except a point between the first and second points, the second inductance element detects a normal mode signal, and the transmitting means injects the phase-inverted signal to the one of the conductor lines, the phase-inverted signal having a phase opposite to a phase of the normal mode signal detected by the second inductance element.

9. The normal mode signal suppressing circuit according to claim 8, wherein the phase-inverted signal transmitting means incorporates a high-pass filter for allowing a normal mode signal to pass there-through.
10. The normal mode signal suppressing circuit according to claim 9, wherein the high-pass filter incorpo-

rates a capacitor.

11. The normal mode signal suppressing circuit according to claim 9, wherein the high-pass filter incorporates a plurality of capacitors that are combined.
12. The normal mode signal suppressing circuit according to claim 8, wherein the impedance element incorporates a third inductance element inserted to the one of the conductor lines.
13. The normal mode signal suppressing circuit according to claim 12, wherein the third inductance element has an inductance of 0.3 μH or greater.
14. The normal mode signal suppressing circuit according to claim 8, wherein a coupling coefficient between the first and second inductance elements is 0.7 or greater.

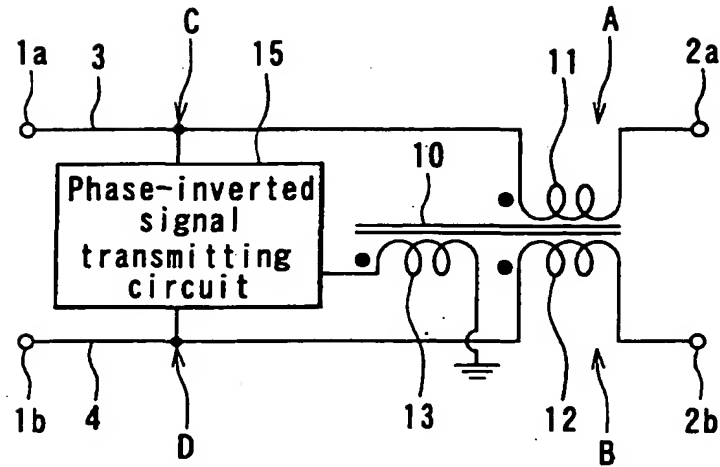


FIG. 1

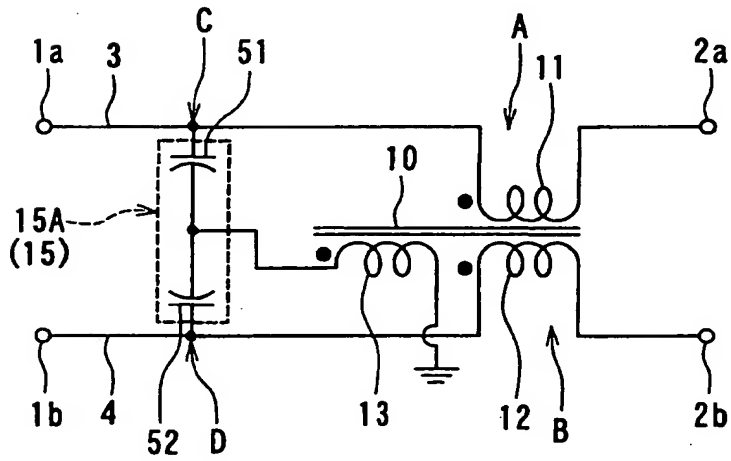


FIG. 2

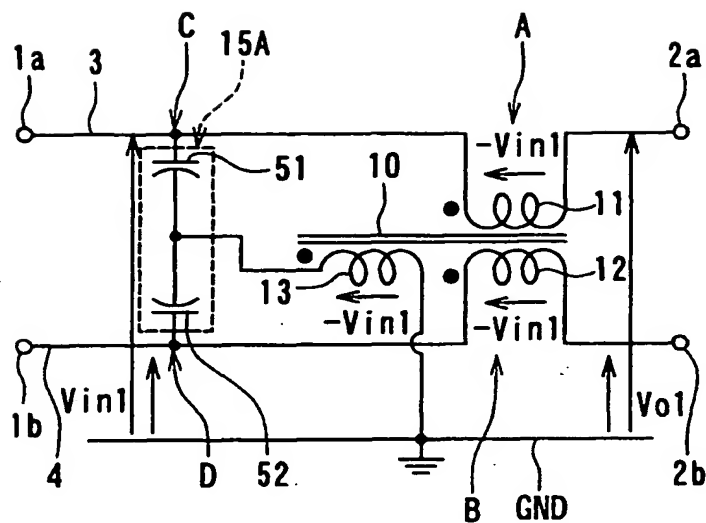


FIG. 3

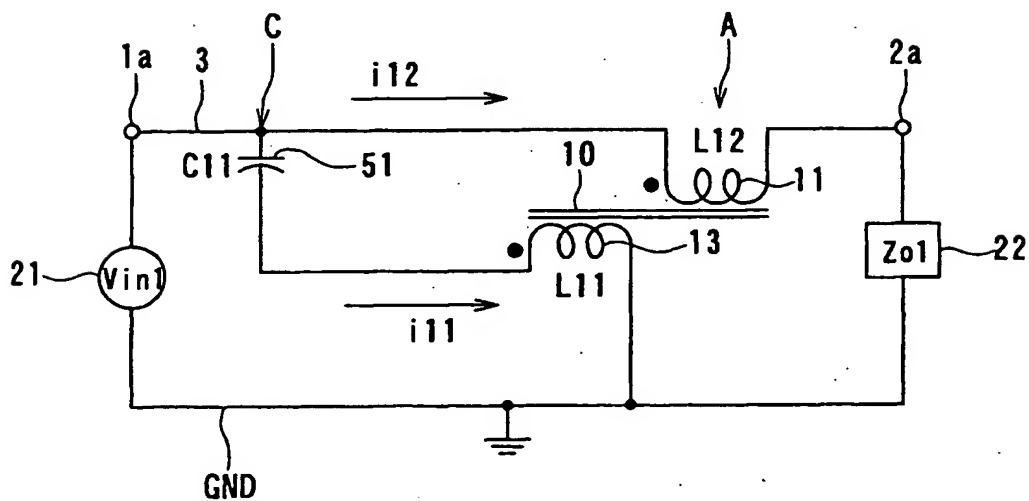


FIG. 4

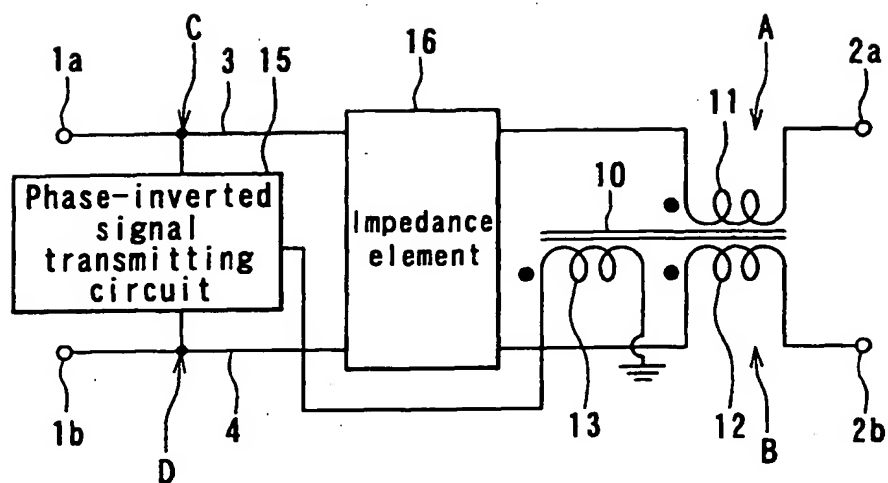


FIG. 5

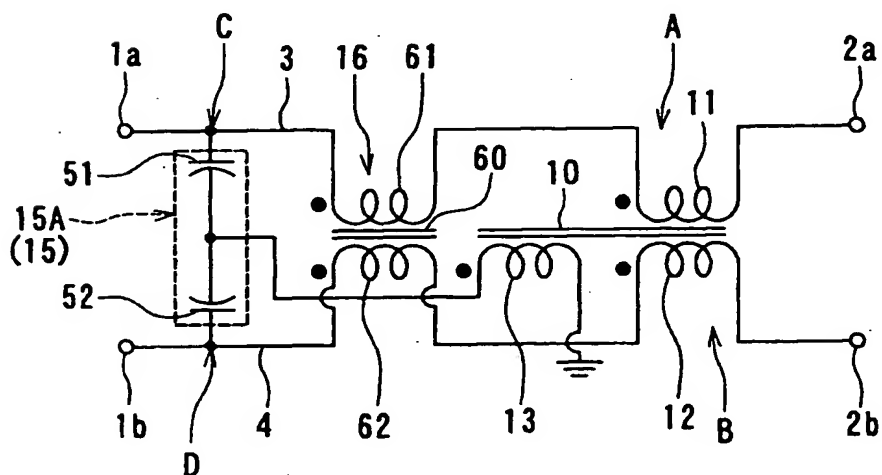


FIG. 6

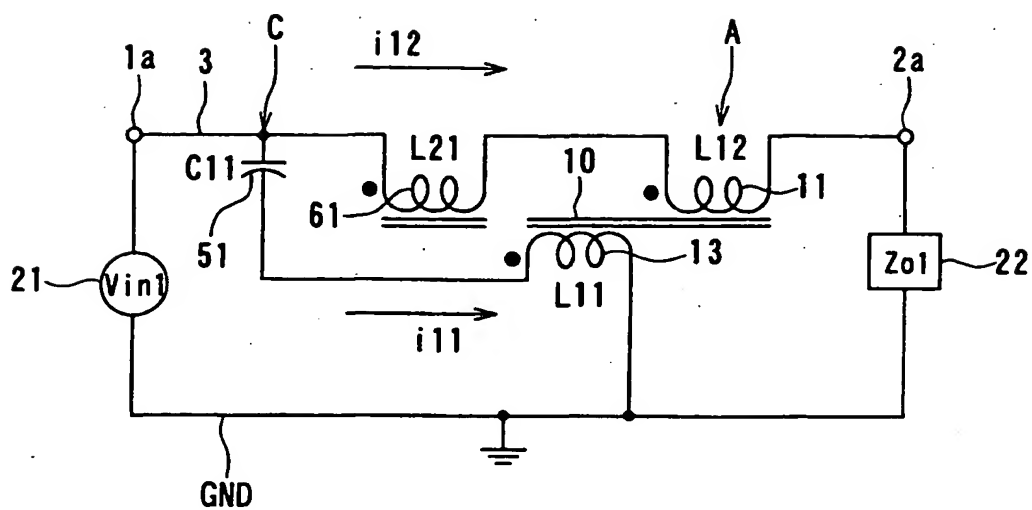


FIG. 7

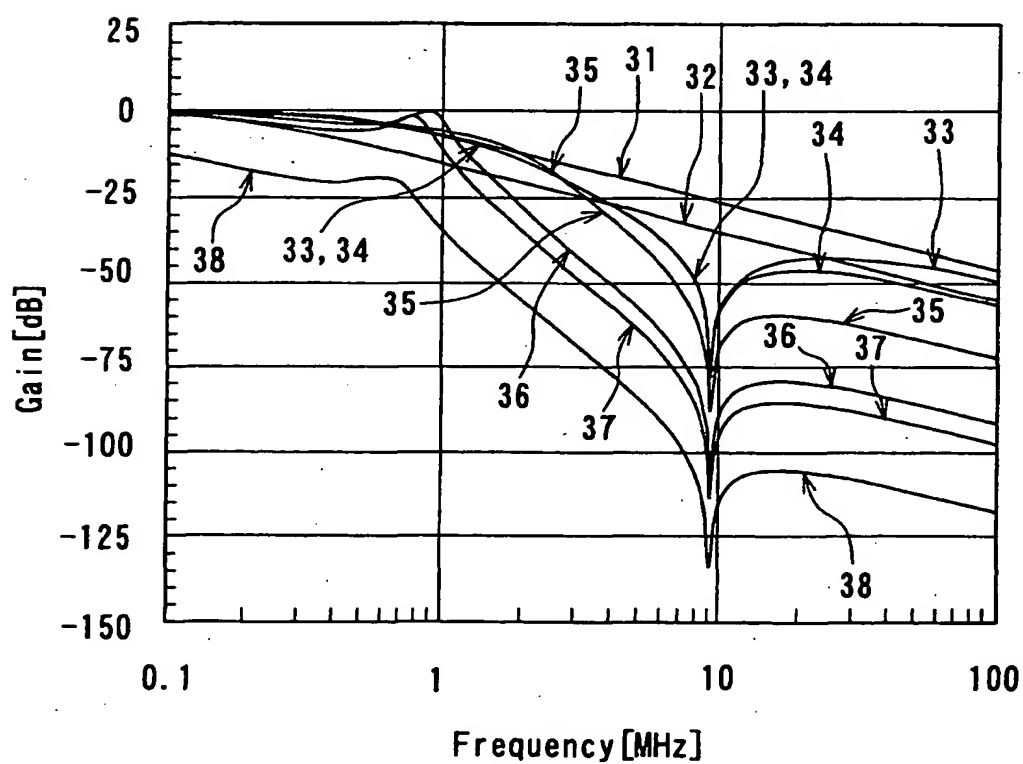


FIG. 8

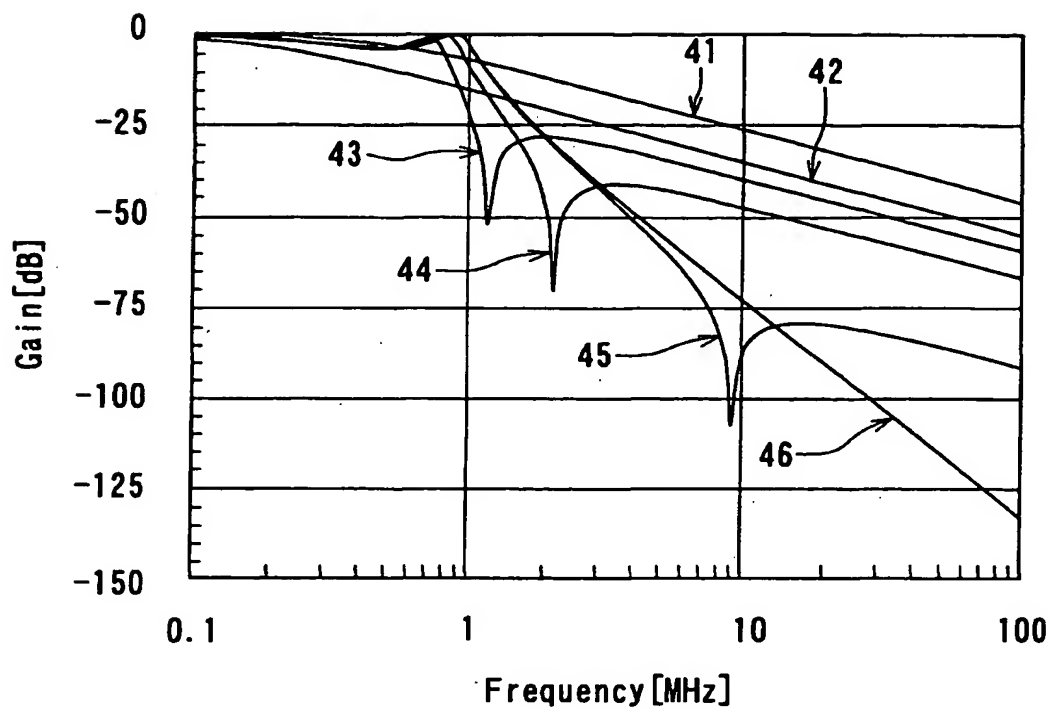


FIG. 9

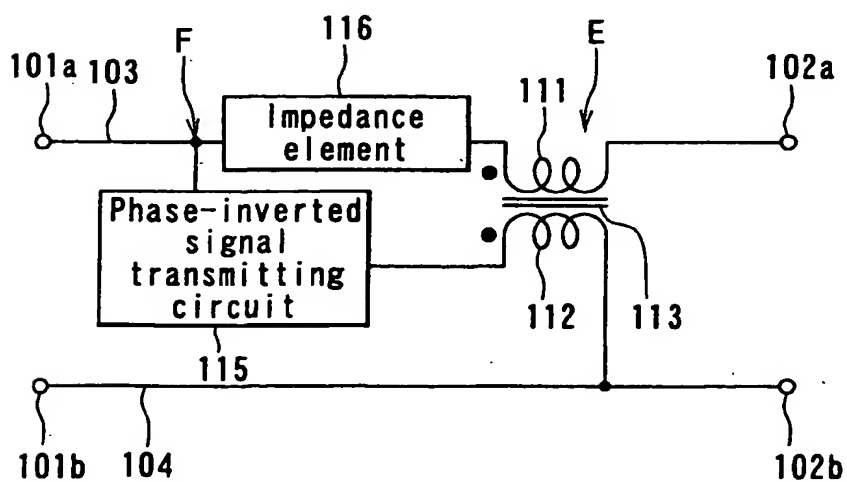


FIG. 10

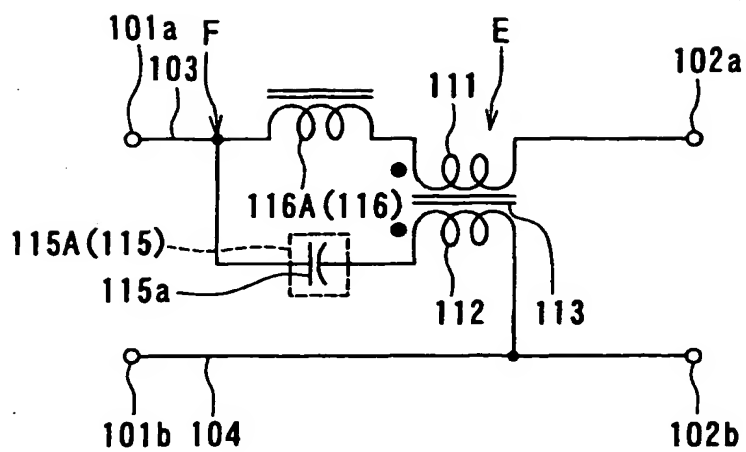


FIG. 11

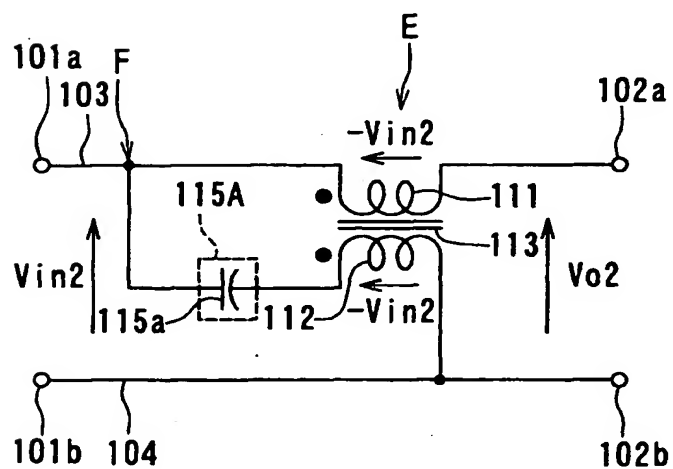


FIG. 12

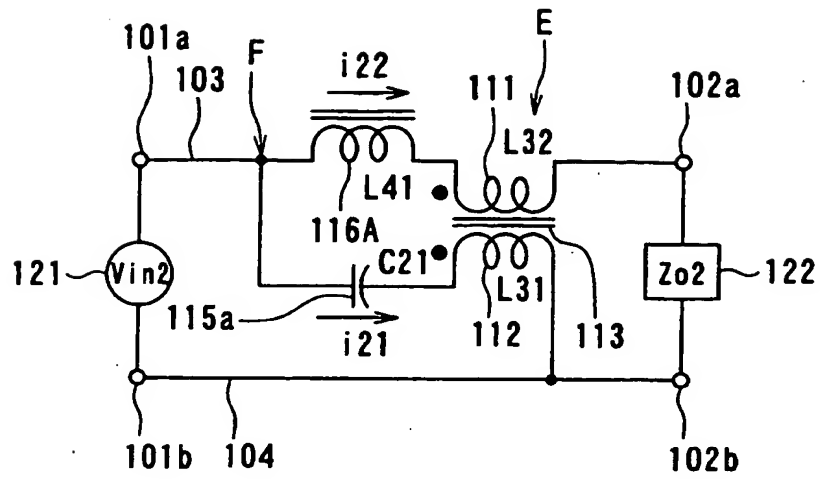


FIG. 13

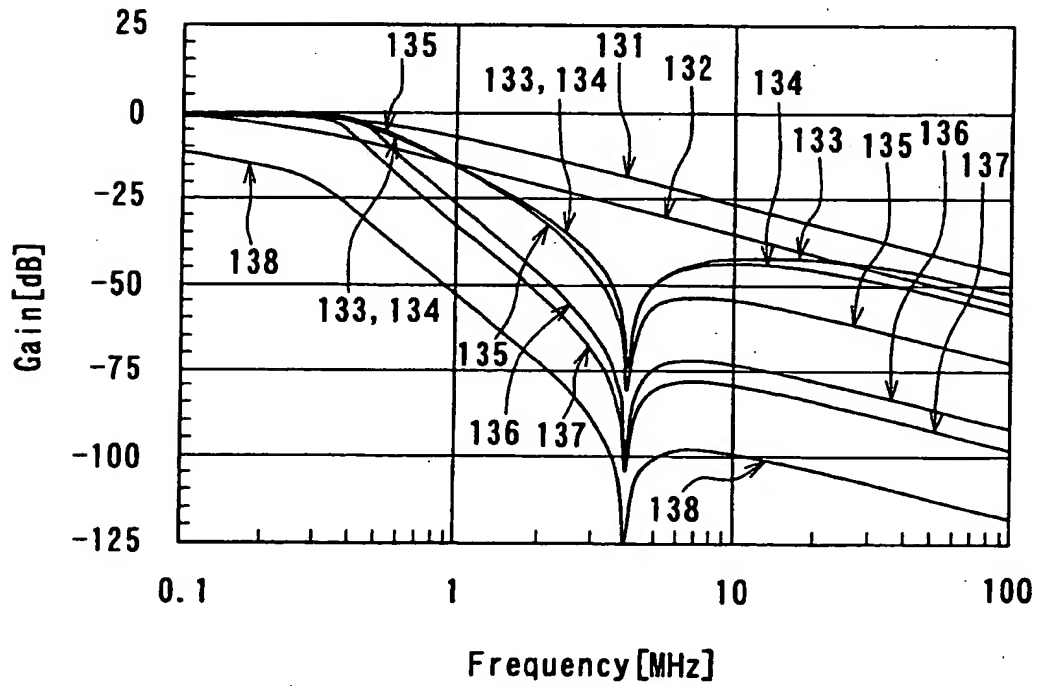


FIG. 14

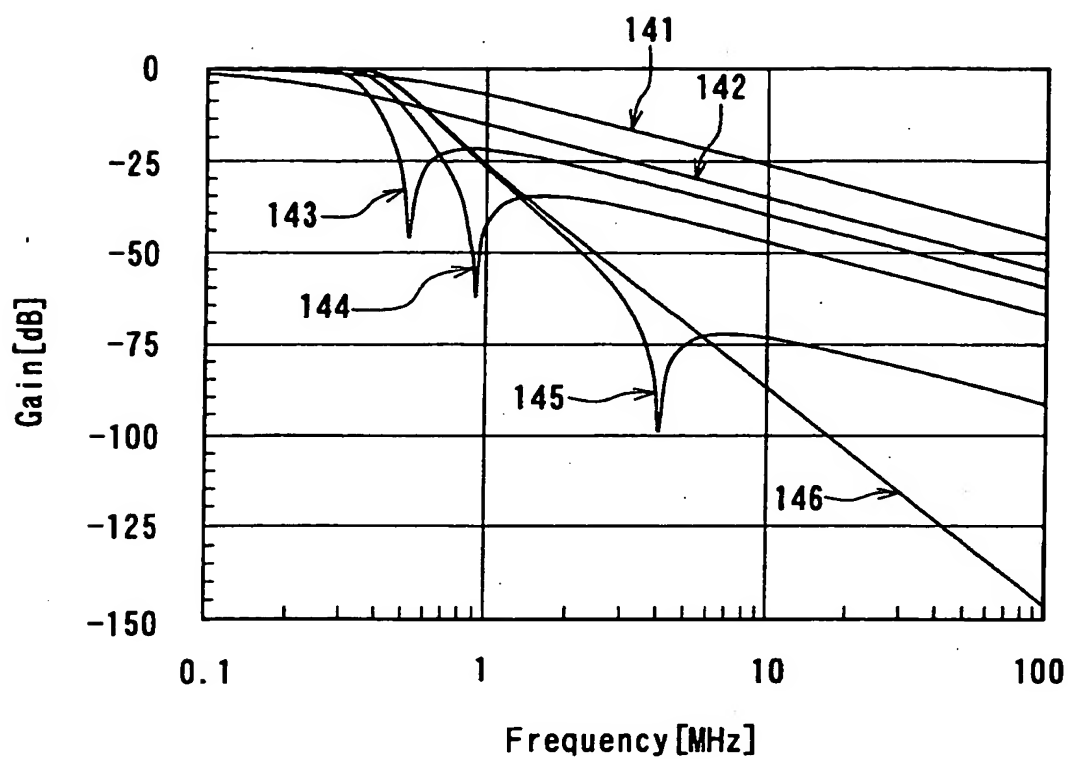


FIG. 15

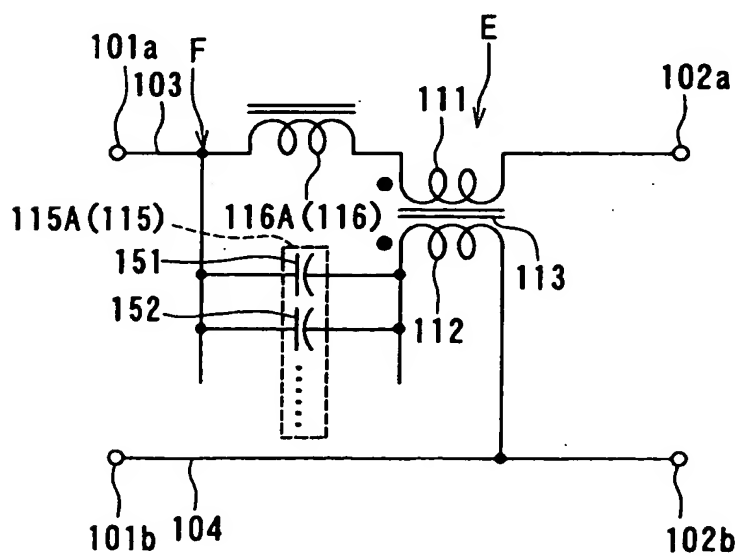


FIG. 16

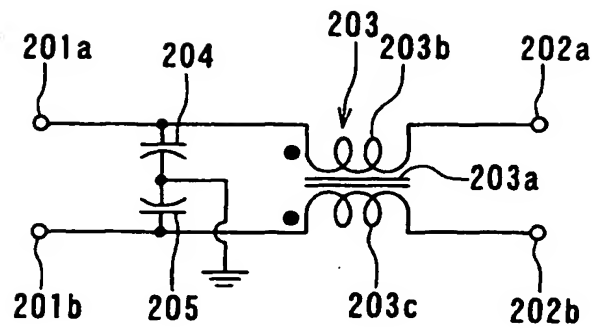


FIG. 17

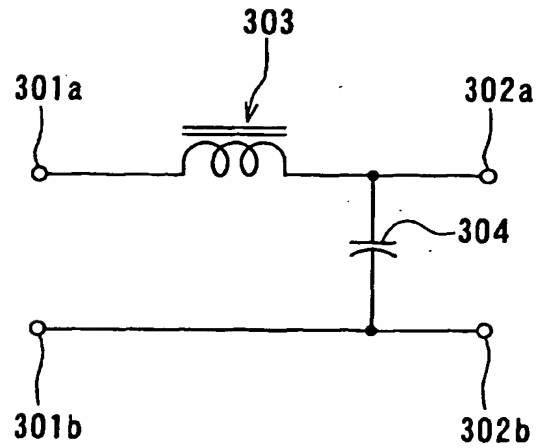


FIG. 18

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP03/10208

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl.⁷ H03H7/09

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl.⁷ H03H7/09Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2003
Kokai Jitsuyo Shinan Koho 1971-2003 Jitsuyo Shinan Toroku Koho 1996-2003Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPI/L

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2002-204189 A (TDK Corp.), 19 July, 2002 (19.07.02), Full text; all drawings & WO 02/37674 A1 & US 2002/0063474 A1 & KR 2002065618 A & EP 1271773 A1 & CN 1394387 A & TW 516270 A	1-14
Y	JP 2000-201044 A (Mitsubishi Electric Corp.), 18 July, 2000 (18.07.00), Full text; all drawings (Family: none)	1
Y	JP 10-303674 A (Sony Corp.), 13 November, 1998 (13.11.98), Full text; all drawings (Family: none)	1, 3, 9

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search
06 November, 2003 (06.11.03)Date of mailing of the international search report
18 November, 2003 (18.11.03)Name and mailing address of the ISA/
Japanese Patent Office

Authorized officer

Facsimile No.

Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP03/10208

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	JP 11-242063 A (NTT Data Corp.), 07 September, 1999 (07.09.99), (Family: none)	1-14
A	JP 11-154843 A (AT & T Corp.), 08 June, 1999 (08.06.99), & US 5844789 A & EP 0902534 A2 & CA 2245803 A1 & CN 1212530 A & MX 9807257 A1	1-14
A	JP 7-22886 A (Yoshihide KANEHARA), 24 January, 1995 (24.01.95), (Family: none)	1-14
A	JP 2-206360 A (Sony Corp.), 16 August, 1990 (16.08.90), (Family: none)	8-14

Form PCT/ISA/210 (continuation of second sheet) (July 1998)